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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/067,410
Filing Date: February 04, 2002
Appellant(s): HILL ET AL.

Brick G. Power
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/8/2007 appealing from the Office action mailed 11/8/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,020,259	Chen et al.	2-2000
5,043,299	Chang et al.	8-1991
5,821,164	Kim et al.	10-1998
6,001,729	Shinrinki	12-1999
5,162,259	Kolar et al.	11-1992

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

9.1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9.2. Claims 1, 8-10, 12-14, 18-20, 23 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6,020,259, submitted by applicant).

In re claims 1, 8, 14, 20, 27 and 28, Chen et al. in Figs. 4-7 and related text, teach the claimed method, comprising:

- causing a chemical reaction (i.e. *TiCl4 reacts with Si*, col. 3, lines 2-19) adjacent to a surface of one exposed, doped area 30 (i.e. source and drain regions) of a semiconductor device structure to *selectively deposit* (col. 3, line 3) titanium silicide or contact material 36 (i.e. $TiSi_2$) by using a *CVD process* (col. 3, line 4) thereon without reacting material of the one exposed, doped area because the formation of the $TiSi_2$ does not consume the underlying doped silicon region 30; and
- subsequently blanket depositing an interconnect material 38 (i.e. a barrier, *TiN*) by using a *CVD process* (col. 3, lines 20 –22) onto the metal silicide or the contact material 36 *after* causing the chemical reaction (col. 3, lines 20-23).

With respect to the interconnect material (TiN) being deposited *in situ* with causing the chemical reaction, Chen et al. do imply a desirability of depositing the interconnect material in situ (i.e. in the same chamber) with causing the chemical reaction because Chen et al. teach depositing the interconnect material 38 and causing the chemical reaction to form titanium silicide with a **same** technique, i.e. the CVD process (col. 3, lines 2-4 and 20-22). Regarding the limitation of "in situ", it is conventional practice to perform as many processing steps in a single apparatus as possible to avoid contamination from the outside atmosphere. Further, apparatus limitations, unless they affect the process in a manipulative sense, may have little weight in process claims. In re Tarczy-Hornoch 158 USPQ 141, 150 (CPPA 1968); In re Edwards 128 USPQ 387 (CCPA 1961); Stalego V. Heymes 120 USPQ 473, 478 (CCPA 1959);

Ex parte Hart 117 USPQ 193 (PO BdPatApp 1957); In re Freeman 44 USPQ 116 (CCPA 1940); In re Sweeney 72 USPQ 501 (CCPA 1947).

Therefore, one of the ordinary skill would have motivated to cause the chemical reaction to selectively deposit metal silicide 36 and deposit the interconnect material 38 onto the metal silicide 36 after and *in situ* with causing the chemical reaction by first providing a silicon-containing ambient (col. 3, lines 5-10) into the CVD chamber; and, *within the same CVD chambe*r, subsequently changing the ambient inside the chamber from silicon-containing to nitrogen-containing (col.3, lines 20-22) to deposit the interconnect material 38. The motivation and suggestion for doing so is to provide a better process for forming the metal silicide and the interconnect material in the same reaction chamber to avoid undesirable contamination from external atmosphere.

In re claims 9, 10, 25 and 26, Chen et al. teach that depositing the interconnect material (TiN) comprises *blanket* depositing the interconnect material (col. 3, lines 20-23) and *patterning* the interconnect material by removing the excess interconnect material from outside of the contact hole (Figs.6-7).

In re claims 12, 13 and 23, Chen et al. further teach depositing an electrically conductive layer 40 over the interconnect material 38 and patterning the electrically conductive layer 40 by removing the excess electrically conductive layer from the outside of the contact hole (Fig.7).

In e claims 18-19, Chen et al. further teach that depositing the interconnect material comprises reacting a metallic precursor (i.e.$TiCl_4$ or titanium tetrahalide) with a reactant comprising an activated species (i.e. N_2) (col. 3, lines 20-24).

9.3. Claims 2-5 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. as applied to claims 1, 8-10, 12-14, 18-20, 23 and 25-28 above, and further in view of Chang et al. (US 5,043,299).

In re claims 2-4 and 21, Chen et al teach the claimed method, as stated above, but fails to teach exposing said at least one exposed, doped area of the semiconductor device structure to a plasma comprising an activated species of at least one of nitrogen, hydrogen, and ammonia; and cleaning the semiconductor device structure.

Chang et al., in an analogous art of selective deposition, teach a pre-deposition preparation by exposing the exposed, doped area of the semiconductor device structure to plasma comprising an activated species of at least one of nitrogen and hydrogen (Fig.1 and text in col. 3, lines 14-26; col. 4, lines 10-15); and cleaning the semiconductor device structure (col.7, lines 1-11) for the purpose of removing contaminants including undesirable oxide and moisture (col.2, lines 15-28; col.6, lines 48-61).

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to expose the exposed, doped area of semiconductor device structure of Chen et al to the plasma comprising either nitrogen or hydrogen; and cleaning the semiconductor device structure, as taught by Chang et al., since by doing so it would be beneficial to the subsequent selective deposition. (col.2, lines 15-28; col.6, lines 48-61, Chang et al)

In re claim 5, Chen et al in view of Chang et al. further teach that said cleaning includes employing a cleaning agent comprising chlorine. Particularly, Chang et al. indicated using a halogen-containing gas, which would include chlorine and fluorine for the cleaning purpose. (col. 7, lines 5-6).

In re claim 22, Chen et al in view of Chang et al. do not teach exposing the semiconductor device structure to a nitrogen-ammonia plasma. However, the selection of the cleaning plasma for said exposing step is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the cleaning plasma can be selected for the particular surface to be cleaned, dependent upon the material of the particular surface. (col. 3, lines 14-26, Chang et al.) In this case, the applicant is required to demonstrate the criticality, generally by showing that the claimed plasma would achieve unexpected results relative to the prior art. See M.P.E.P. 2144.05 III.

9.4. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. as applied to claim 1 above, and further in view of Kolar et al. (US 5,162,259).

Chen et al. teach the claimed method, as stated above, but fails to teach cleaning the semiconductor device structure after said depositing said metal silicide, wherein said cleaning includes employing a cleaning agent comprising at least one of chlorine, hydrochloric acid, and hydrofluoric acid.

Kolar et al. in an analogous art teach forming a silicide layer 40 followed by cleaning the semiconductor device structure employing a cleaning agent comprising hydrochloric acid, prior to depositing an interconnect material 38. (Fig.4 and text in col. 21-23)

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to utilize said hydrochloric acid as cleaning agent as taught by Kolar et al.,

in the method of Chen et al. to clean the surface of said deposited metal silicide; and then to deposit said interconnect material, since by doing so it would improve the adhesion between adjacent layers.

9.5. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. as applied to claim 1 above, and further in view of Kim et al. (US 5,821,164).

Chen et al. do not teach *selectively* depositing the interconnect material (TiN).

However, using selective deposition for forming TiN in a contact hole has been widely used in the art, as evidenced by Kim et al. (col. 4, lines 24-27). Kim et al. teach selectively depositing the interconnect material 16 (col. 4, lines 24-27), such as TiN, in a contact hole 15 (Figs. 2E~2F).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to use the selective deposition, as taught by Kim et al., for forming the interconnect material of Chen et al, since by this manner it would provide a better means for controlling the desired depositing location and thickness of the interconnect material.

9.6. Claims 15-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. as applied to claim 1 above, and further in view of Shinriki et al. (US 6,001,729).

Chen et al. teach that causing the chemical reaction comprises reacting a metallic precursor (i.e. *$TiCl_4$ or titanium tetrahalide*) with silicon (col. 3, lines 2-19) but is silent as to the silicon source being a silicon compound.

Shinriki et al., however, teach causing a chemical reaction via reacting metallic precursor (i.e. $TiCl_4$) with a silicon compound (i.e. SiH_4 or silane) (col. 12, lines 37-39) adjacent to a

surface of one exposed, doped area 38 of a semiconductor device structure to selectively deposit titanium silicide.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to use the silicon compound, as taught by Shinriki et al., as the silicon source of Chen et al., since by this manner it would satisfactorily cause the chemical reaction to form the titanium silicide.

(10) Response to Argument

The major issue in the arguments is whether or not it is obvious to one of the ordinary skill in the art, at the time of the invention was made, to apply Chen's teachings (US '259) to depositing an interconnect material onto the metal silicide **in situ** (i.e. in the same reaction chamber) with causing the chemical reaction that is used for selectively depositing metal silicide.

In this regard, Appellants asserted that " there is no reason that one skilled in the art would be expected to draw the inference that separate chemical reactions with different reactants would take place in the same reaction chamber simply because chemical vapor deposition (CVD) processes are used to effect both reactions." (third paragraph, page 8) Appellants further argued that " teaching that CVD may be used to deposit different layers on a semiconductor implies nothing other than that a certain type of process, with different reactions at discrete points in time, may be used to form layers of different materials" and that " without actually teaching or suggesting that the two reactions of Chen are effected in the same chamber, or in situ, one cannot imply anything more from the disclosure of Chen." (third paragraph, page 8) Thus, appellant

maintained that "different material layers have conventionally been formed in different reaction chambers, even if the same general process (*e.g.*, CVD) was used form both material layers." (third paragraph, page 8)

In respond to the foregoing arguments, Chen et al. teach introducing reactant $TiCl_4$ in the Si ambient, via CVD technique, causing a chemical reaction (i.e. $TiCl_4 + Si \dashrightarrow TiSi_2$) to selectively deposit metal silicide 36 (i.e. $TiSi_2$) (col. 3, lines 1-15). Then, Chen et al. still introduce the same reactant $TiCl_4$, via the same CVD technique, and subsequently switch the ambient from Si to nitrogen (col. 3, lines 20-21) to deposit an interconnect material TiN layer 38 (col. 3, line 22) onto the metal silicide $TiSi_2$ layer 36 (Fig.6) after causing the chemical reaction (i.e. $TiCl_4 + Si \dashrightarrow TiSi_2$).

Chen et al. is silent as to the step of depositing the interconnect material (i.e. $TiSi_2$) being **in situ** with causing the chemical reaction (i.e. depositing TiN). In other word, Chen et al do not expressly teach that forming both $TiSi_2$ and TiN are performed in the same CVD reaction chamber.

Regarding the limitation of "in situ", it is conventional practice to perform as many processing steps in a single apparatus as possible to avoid contamination from the outside atmosphere. Further, apparatus limitations, unless they affect the process in a manipulative sense, may have little weight in process claims. In re Tarczy-Hornoch 158 USPQ 141, 150 (CPPA 1968); In re Edwards 128 USPQ 387 (CCPA 1961); Stalego V. Heymes 120 USPQ 473, 478 (CCPA 1959); Ex parte Hart 117 USPQ 193 (PO BdPatApp 1957); In re Freeman 44 USPQ 116 (CCPA 1940); In re Sweeney 72 USPQ 501 (CCPA 1947).

Consequently, one of the ordinary skill would have motivated to first using CVD technique to selectively deposit metal silicide 36 and then using the same CVD techniques to deposit the interconnect material 38 onto the metal silicide 36 in the **same** CVD reaction chamber by simply changing the ambient inside the reaction chamber from silicon-containing ambient to nitrogen-containing ambient (col.3, lines 20-22). The motivation and suggestion for doing so is to provide a simple process for forming both the metal silicide and the interconnect material in situ, without changing into separate chamber, to avoid undesirable contamination from external atmosphere.

Performing similar processing steps in situ is a well-known practice in the art to eliminate undesirable external contamination, as stated previously. Particularly, in Chen's teachings, the only difference in processing step between depositing metal silicide 36 (i.e. $TiSi_2$) and depositing interconnect material 38 (i.e. TiN) is the ambient. The ambient in depositing metal silicide is silicon ambient (col. 3, line 7, Chen et al.), whereas in depositing the interconnect material is nitrogen ambient (col. 4, line 21, Chen et al.). Thus, it would have been obvious to one of the ordinary skills in the art, to **maintain in the same CVD chamber** after depositing the metal silicide 36, then to purge the chamber and subsequently *switching from silicon ambient to nitrogen ambient* to proceed the step of depositing the interconnect material 38 (i.e. TiN). It is well known that the major advantages for performing deposition **in situ** are preventing external contamination and simplifying processing steps. Therefore, Appellants' assertion of "different material layers have conventionally been formed in different reaction chambers, even if the same general process wad used form both material layers" is not persuasive.

Regarding Chen in view of Chang, Appellant argued that "neither Chen nor Chang, taken together or separately, teaches or suggests exposing a semiconductor structure to a nitrogen-ammonia plasma." (last paragraph, page 10)

In response to the argument, Chang suggested that the selection of the plasma gas for cleaning purpose is material-to-be-cleaned dependent (col. 3, lines 14-26). One of the ordinary skills in the art would have motivated to expose the semiconductor device to a preferred plasma that is effective to remove undesirable residues from the surface of the semiconductor device structure without compromising the integrity of the semiconductor device. In this case, Appellants have not demonstrated that exposing the semiconductor device structure to a nitrogen-ammonia plasma would achieve unexpected results.

Regarding Chen in view of Kolar, Appellants do not clearly point out why the rejection is improper. (second paragraph, page 11)

Regarding Chen in view of Kim, Appellants maintained that "the formation of conductive layer 16 must be followed by an etch-back, as explained at col.4, lines 28-31 of Kim" and therefore, "deposition of the conductive layer 16 would certainly not be selective." (first paragraph, page 12).

In response to the foregoing argument, Kim clearly discloses that " a material among Al, Cu, Ti and TiN is **selectively** deposited on the exposed surface of the interlevel layer **14a** including the contact hole **15**, to form a conductive layer **16**." (Emphasis added) (col. 4, lines 24-27, Kim) Obviously, the conductive layer 16 is **selectively** deposited. The reason why Kim teaches that the conductive layer 16 is selectively removed by a photolithography and etching step or etch-back process, to form a second line 16 (col. 4, lines 28-30, Kim) is because, even

using selective deposition for fully filling the contact hole 15 with the conductive layer 16, it still has a portion of layer 16 being deposited outside of the contact hole 15 on the surface of the interlevel layer 14a. Therefore, the etch-back is needed to remove the undesirable portion of layer 16 from the surface of the interlevel layer 14a in order to form the second line 16 which resides only within the contact hole 15, as taught by Kim in col. 4, lines 28-30. Kim, however, **does** teach using **selective** deposition for forming the conductive layer 16, as stated in col. 4, lines 24-27. Appellants, apparently misinterprets Kim's teachings and assumed that as long as etch-back process is involved, then the deposition must be non-selective. Unfortunately, it is not always true. And, Kim's teachings demonstrated that even using selective deposition, etch-back processing step still got involved in order to form a conductive line only in the contact hole.

Appellant further argued that "Chen also lacks any teaching or suggestion of selectively depositing an interconnect material." (second paragraph, page 12).

In response to Appellants' argument against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Regarding Chen in view of Shinriki, Appellants do not clearly point out why the rejection is improper. (last paragraph, page 12)

Respectfully submitted,

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